A PLANAR CIRCUIT DESIGN FOR HIGH ORDER SUB-HARMONIC MIXERS

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Abstract **- A planar circuit design technique is presented that results in relatively low conversion loss for sub-harmonic mixers using high-order LO harmonic frequencies. The design method results in conversion losses from 15 to 20 dB for LO frequencies ranging from the 3rd to the 9th sub-harmonic for signal frequencies up to W-Band. Measured data agrees closely to the simulated results for a 25 GHz, 3rd and 5th sub-harmonic prototype. The resulting conversion loss of these designs is not sensitive to the harmonic number used and provides an simple, commercially viable, planar approach to high frequency mixer designs.**

I. Introduction

Sub-harmonic mixers at very high frequencies have the advantage over their fundamental frequency counterparts in that they do not require high power, high frequency local oscillator (LO) sources. As the frequency requirement increases, quality oscillators with the stability and power levels required for proper mixing are either prohibitively expensive or are simply not available. Mixers designs that can use a sub-harmonic of the signal's fundamental frequency can operate at high signal frequencies and still use the low frequency oscillators available in the sub-harmonic frequency range for down-conversion. The price normally paid for this technique is a large increase in conversion loss as the sub-harmonic frequency number is increased. Some commercially available waveguide based sub-harmonic mixers list conversion losses at W-band from 20 to 40 dB (and higher) depending upon which sub-harmonic pump frequency is chosen. The large increase in conversion loss as the LO frequency is lowered provides a practical lower limit on the minimum sub-harmonic frequency that can be used.

In this work a design method is presented that uses a number of circuit design techniques including conjugate and "match-point" impedance mapping [1,2,3], which, when combined properly, result in high-order sub-harmonic mixers with conversion loss under 20 dB for RF signal frequencies up to W-Band and beyond.

II. Design Procedure

The first step in the design procedure is to determine the input impedance to the diode (which is connected in shunt to ground) for both the "on" and "off" states. These impedance's can be approximated using the

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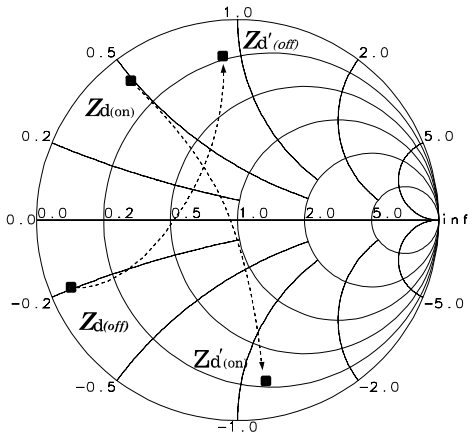

Figure 1. Diode state impedance mapping (Zd = state before matching, Zd' = state after mapping) .

diode parameters (Rs, Cj, ect.) [3], or they can be obtained more accurately using a harmonic balance circuit simulator. The advantage of the circuit simulator is that the impedance of the diode *including* all of the embedding structures can be obtained. The measured or calculated impedance states can then be used to calculate the "hyperbolic mean" [3] or "match point" impedance[1] which is then conjugate matched to the system impedance. This results in having the "on" and "off" states of the diode being mapped into two points on the Smith chart spaced as far apart as possible and being 180° out of phase (Figure 1).

A combination of transmission lines (90° at the RF frequency) are used to provide a path for the LO and IF signals that is isolated from the diode and its RF matching circuitry. The LO signal is then conjugate matched into the diode to provide the time-varying bias voltage required to switch the diode impedance states. The LO port also contains a Band-Pass Filter (BPF) to isolate the LO port from the resulting IF signal, which is extracted through a Low-Pass Filter (LPF). A length of transmission line (90° at the LO frequency) is placed between the diode and the LPF, which is designed with a leading shunt capacitor to provide a short-circuit to high frequency signals. This places an effective open circuit at the plane of the diode to the LO fundamental frequency and all odd harmonics, with even harmonics being terminated in a short circuit (the RF matching circuit is small compared to the LO frequency and is neglected). The resulting circuit design is shown in Figure 2. The harmonic balance simulator can now be used to adjust the RF matching circuit (to compensate for the effects of the IF and LO circuitry) for optimum circuit performance.

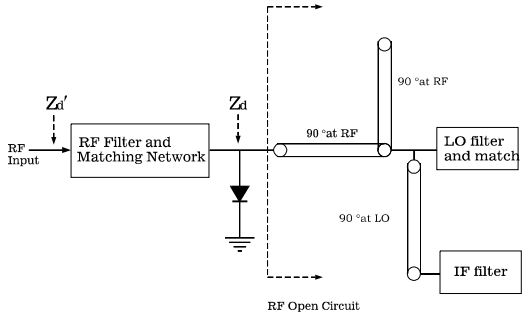

Figure 2. Circuit diagram for planar sub-harmonic mixer.

III. Design Performance

The advantage that these designs hold is that the conversion loss is a relatively weak function of the sub-harmonic pump frequency. The design procedure was repeated for several different LO frequencies (3^{rd}, 5^{th}, and 7^{th} LO Harmonic) with the RF frequency kept at a fixed value. The predicted conversion loss for the designs are shown in Figure 3. As is clear from the graph, the conversion loss can remain nearly constant across a very wide range of pump frequencies.

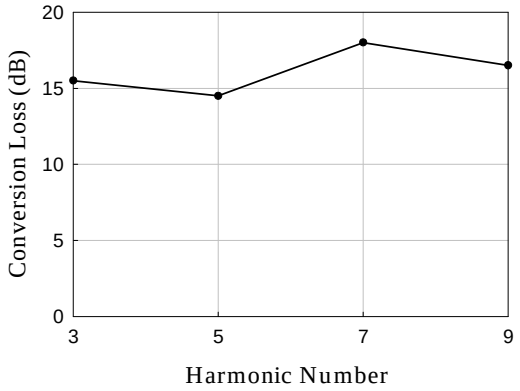

Figure 3. Predicted conversion loss vs. LO sub-harmonic frequency.

A 25 GHz, 5th sub-harmonic mixer prototype was chosen to verify the performance predicted by the harmonic balance circuit simulation. The design procedure was followed and the resulting circuit was fabricated and assembled by hand on a 15 mil Duroid [5] substrate. The RF frequency was chosen based on available measurement resources, and the 5th sub-harmonic LO was chosen for good LO-IF isolation, as the two frequencies can converge when high-order sub-harmonic pump frequencies are used. The mixer conversion loss was measured with the results showing good agreement with the predicted values (Figure 4). The difference between the simulated and measure response is attributed to the modeling of the via connection to the ground plane, which was fabricated with less inductance than what was modeled.

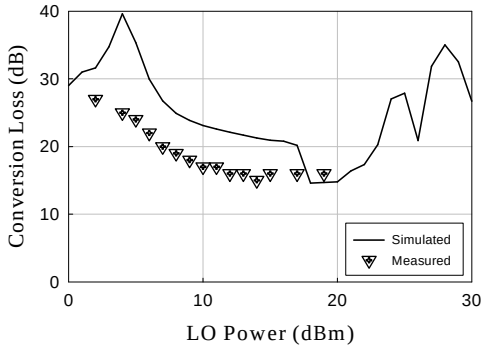

Figure 4. Measured and predicted conversion loss for the 5th sub-harmonic mixer. F_rf = 25 GHz , F_lo = 5 GHz and F_if = 270MHz.

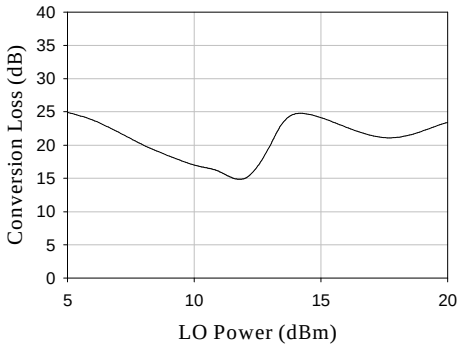

Figure 5. Simulated mixer performance for a monolithic 94 GHz , 9th sub-harmonic mixer.

It is important to note that the conversion loss, both simulated and measured, is for a design using a beam-lead Schottky diode, whose packaging parasitics are a dominate limitation in the mixer‘s performance. Better performance can be obtained when using an integrated diode and MMIC fabrication technology. A 94 GHz, 9th sub-harmonic mixer (F_{LO} = 10 GHz, F_{IF} = 4 GHz) was designed and simulated in the same manner as the measured 5th sub-harmonic design, with the resulting simulated performance shown in Figure 5.

It is expected that the measured results from the completed W-band monolithic mixer will agree as closely to the predicted response as the 25 GHz prototype 5th sub-harmonic did.

IV. Bandwidth Response

The mixers designed and tested during this work were not optimized for wide-band performance. The RF input sections were designed for single input frequency. The

simulated response for an RF frequency ranging from 94 GHz to 95 GHz (IF frequency up to 1 GHz) is shown in Figure 6. The results show a usable SSB bandwidth of about 700MHz at W band when designed for a single frequency. The match procedure can be altered to provide more bandwidth by computing and matching the hyperbolic mean impedance at more than one RF frequency.

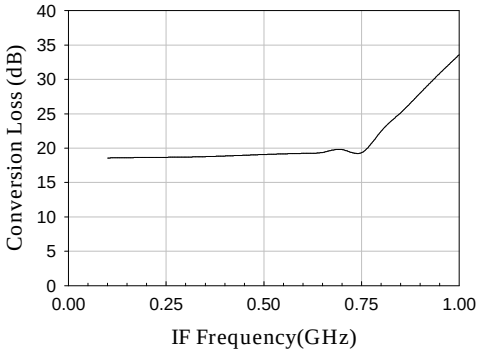

Figure 6. Simulated bandwidth performance for a 94 GHz 9th sub-harmonic mixer matched at a single frequency.

V. Conclusion

A method has been presented that can be followed for the design of sub-harmonic mixers. The design procedure, as well as the resulting conversion loss, is virtually independent of harmonic number (for n odd). The resulting planar circuit displays significantly less conversion loss that commercially available waveguide based products, and will allow for the inexpensive production of high performance monolithically integrated sub-harmonic mixers for high frequency applications.

V. Acknowledgments:

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[3] Bahl and Bhartia, “Microwave Solid State Circuit Design”, Wiley & Sons, 1988

[4] HP EESof Series IV LIBRA- Microwave Circuit Simulation

[5] Duroid is a registered trademark of Rogers Corporation.